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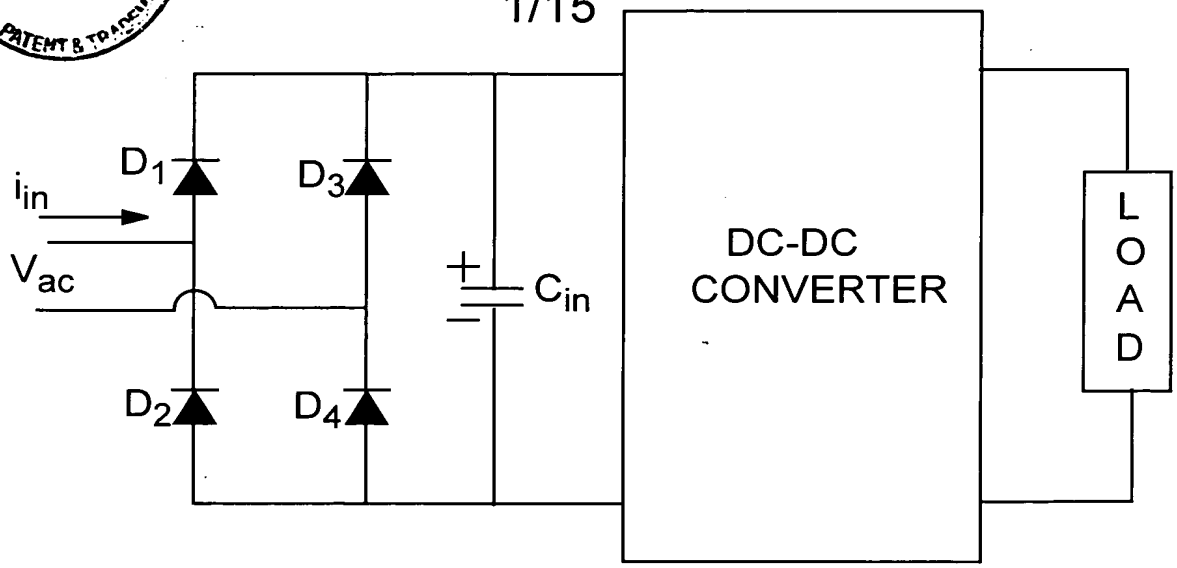
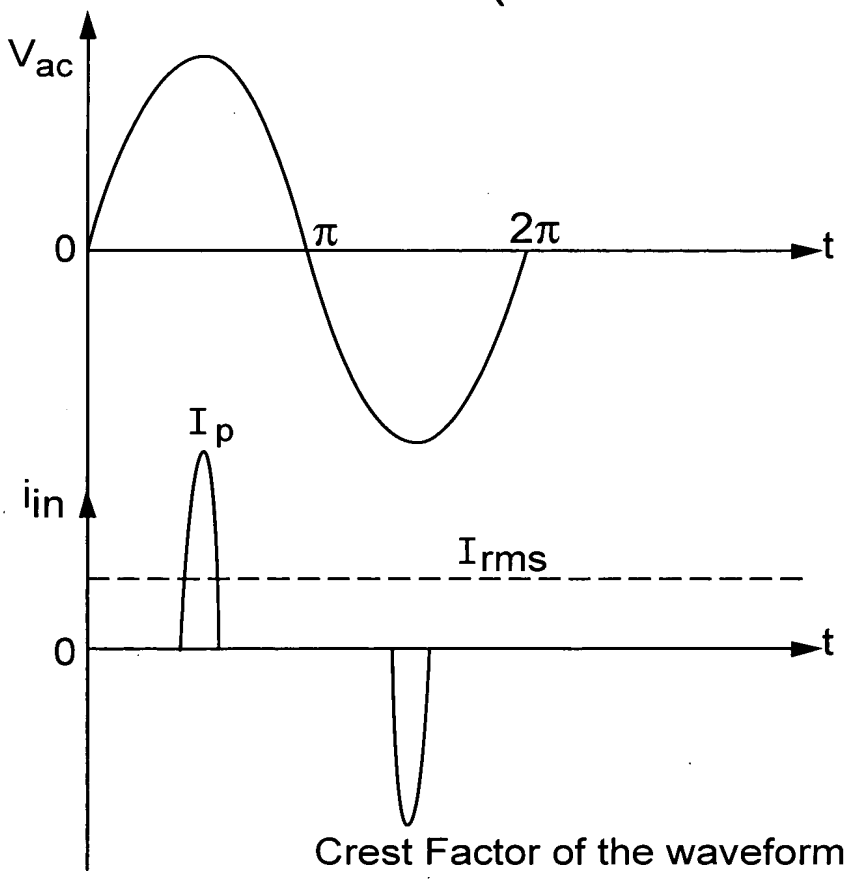


FIG. 1A (PRIOR ART)



$$\text{Crest Factor of the waveform} = \frac{I_p}{I_{rms}}$$

FIG. 1B (PRIOR ART)

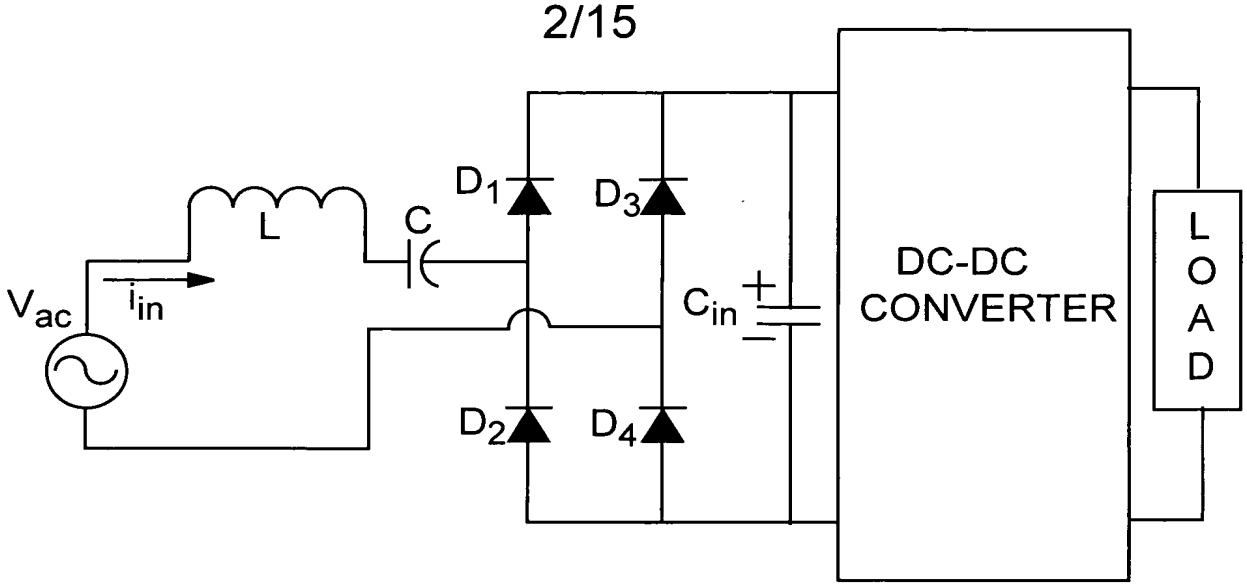


FIG. 2 (PRIOR ART)

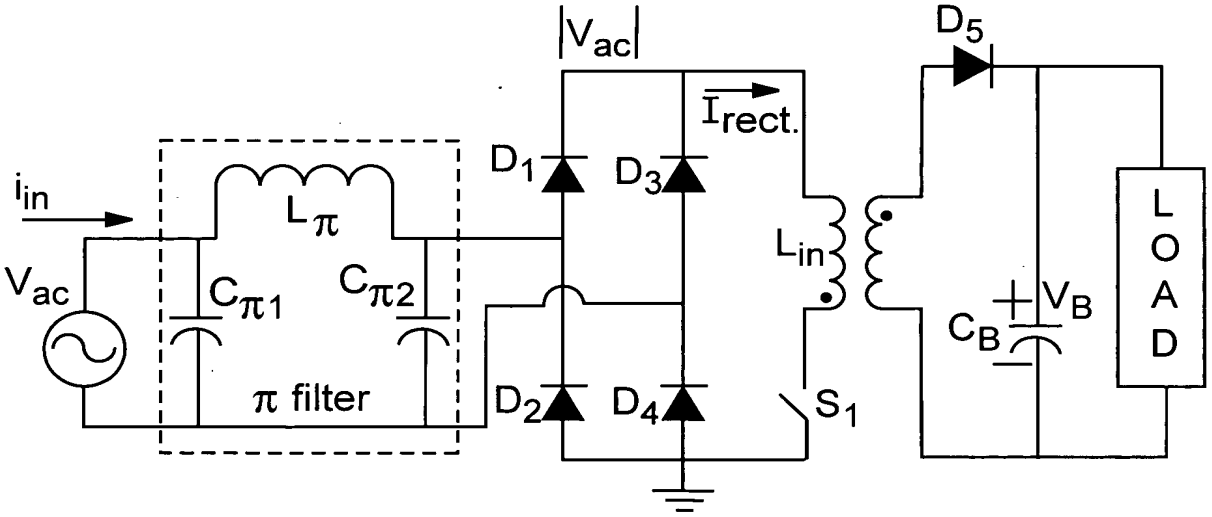


FIG. 3 (PRIOR ART)

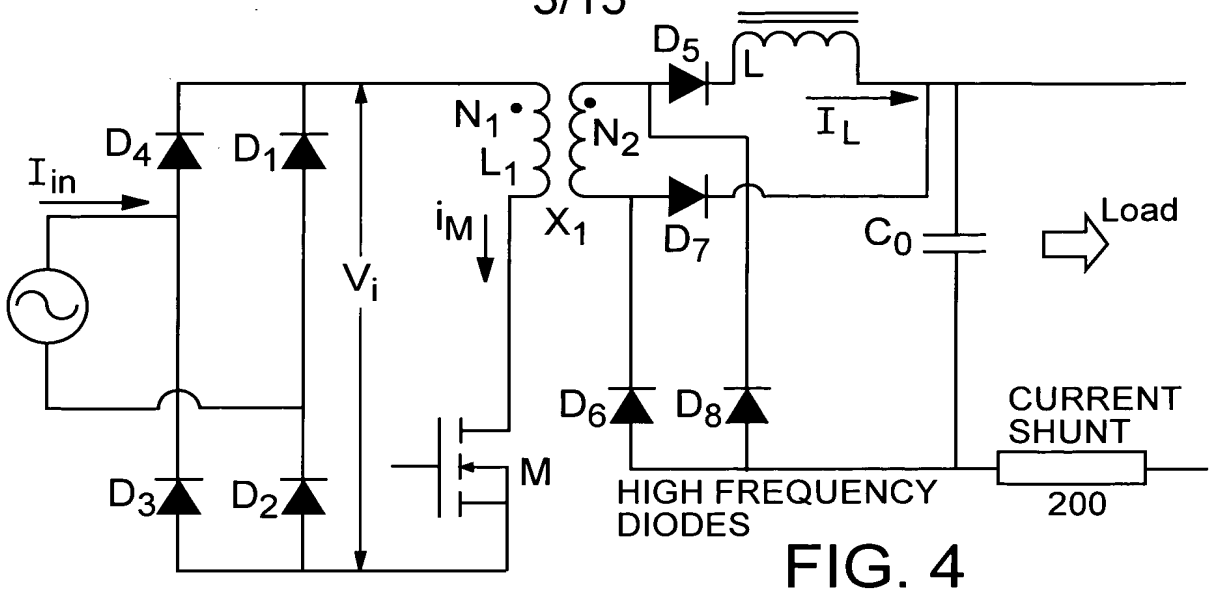


FIG. 4

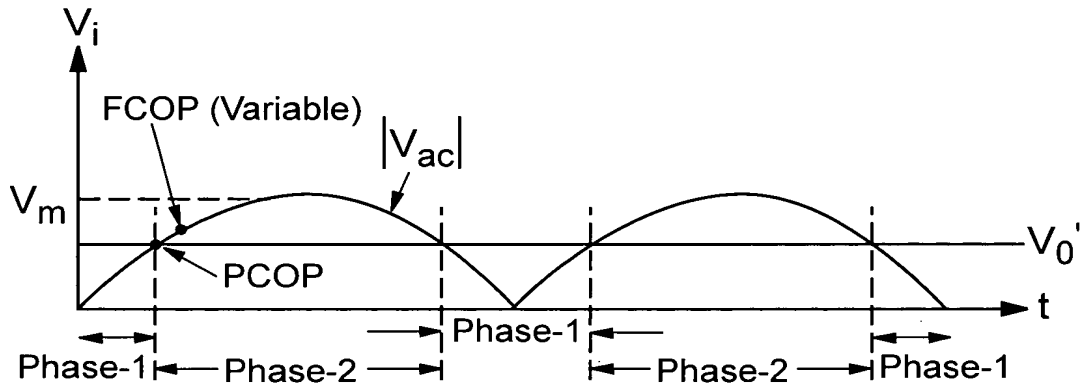


FIG. 5

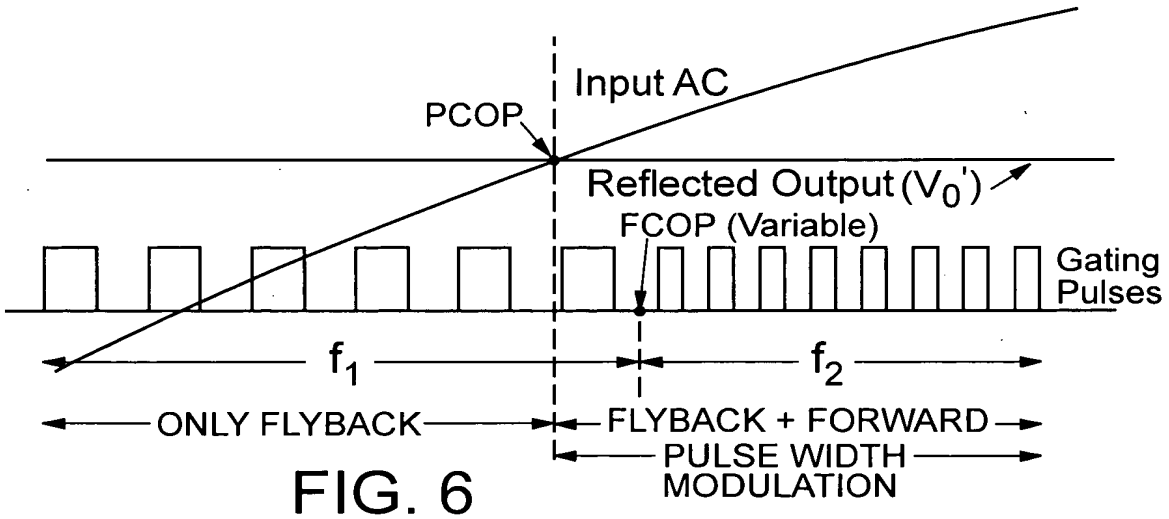


FIG. 6

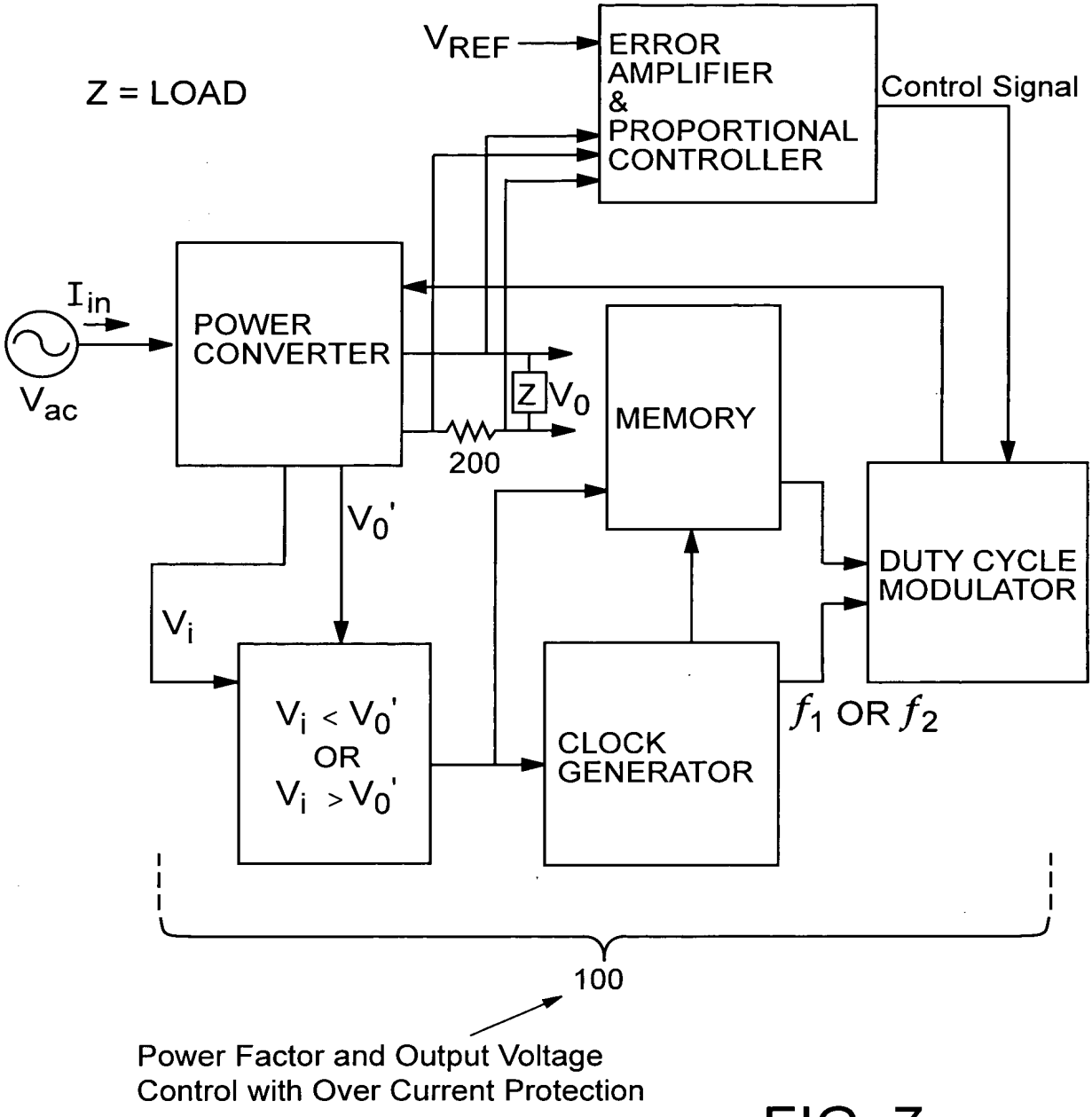

V_{REF}
ERROR AMPLIFIER & PROPORTIONAL CONTROLLER
Control Signal
Z = LOAD
I_{in}
V_{ac}
POWER CONVERTER
Z
V_0
200
MEMORY
V_0'
V_i
DUTY CYCLE MODULATOR
$V_i < V_0'$ OR $V_i > V_0'$
CLOCK GENERATOR
f_1 OR f_2
100
Power Factor and Output Voltage Control with Over Current Protection

FIG. 7

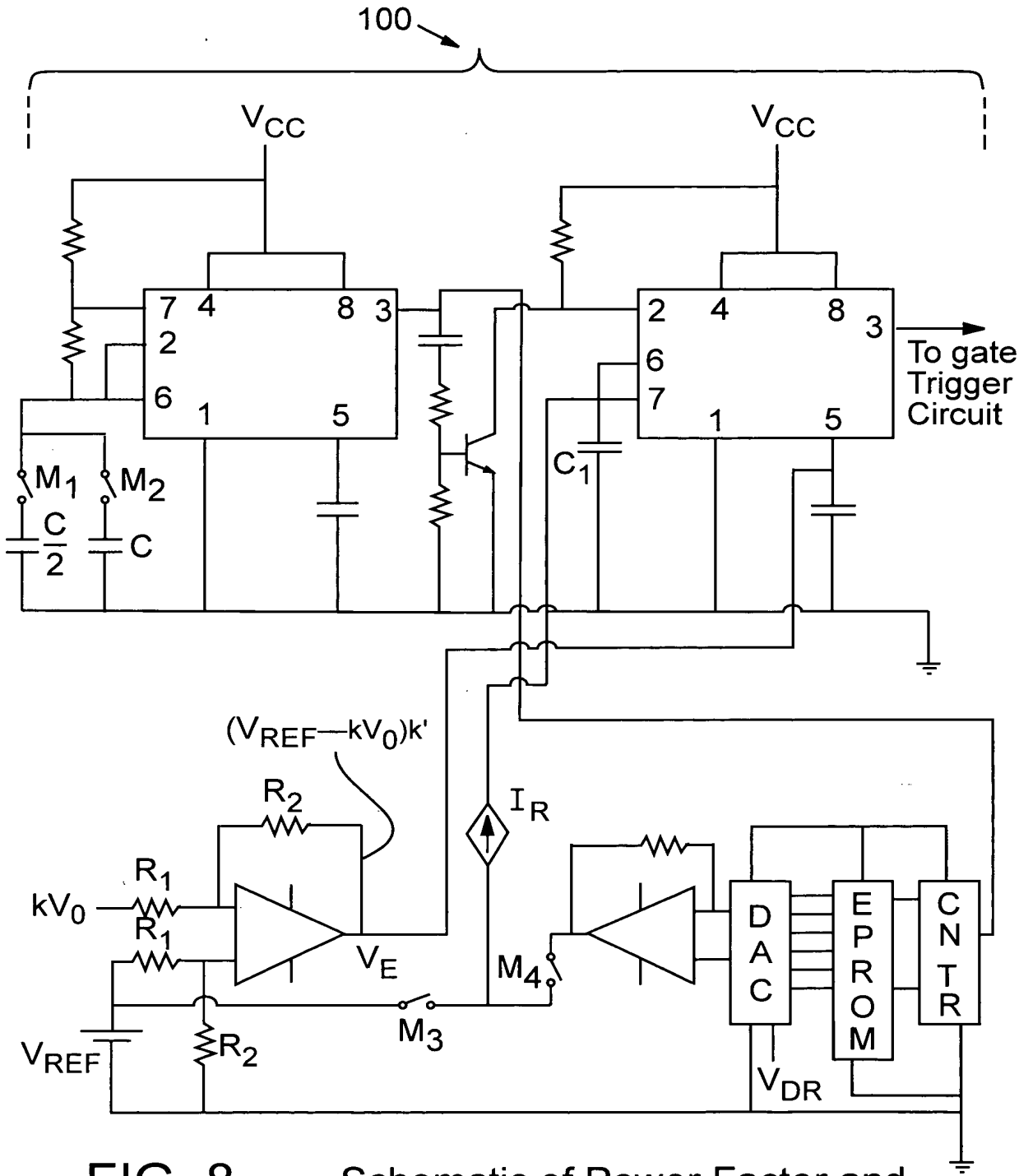
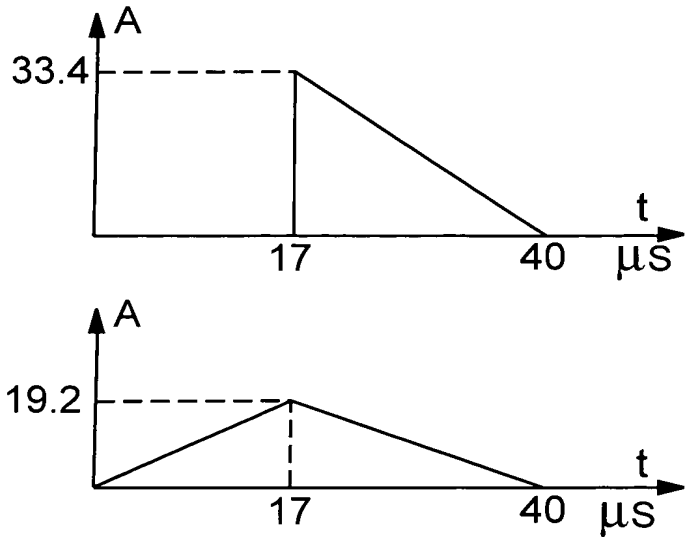


FIG. 8 Schematic of Power Factor and Output Voltage control



	Average Current	RMS Current
Flyback Mode	9.6A	14.7A
Proposed Hybrid Topology	9.6A	11A

Secondary current waveforms

Hybrid technology helps significantly to reduce both peak and RMS currents

FIG. 9 The secondary current waveforms for a flyback converter and hybrid technology

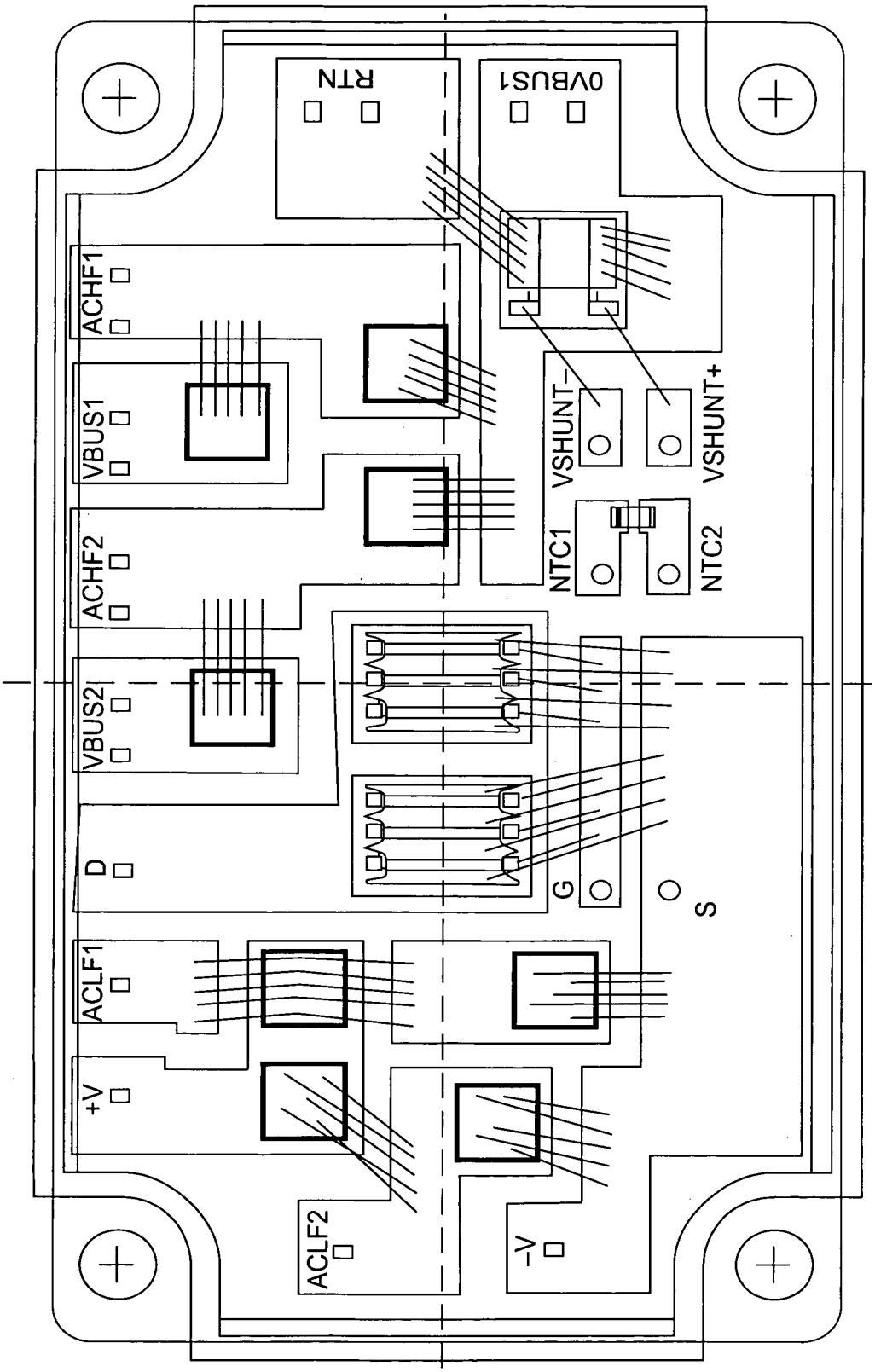


FIG. 10A POWER MODULE – LAYOUT
SMART CONVERTER MODULE – POWER STAGE

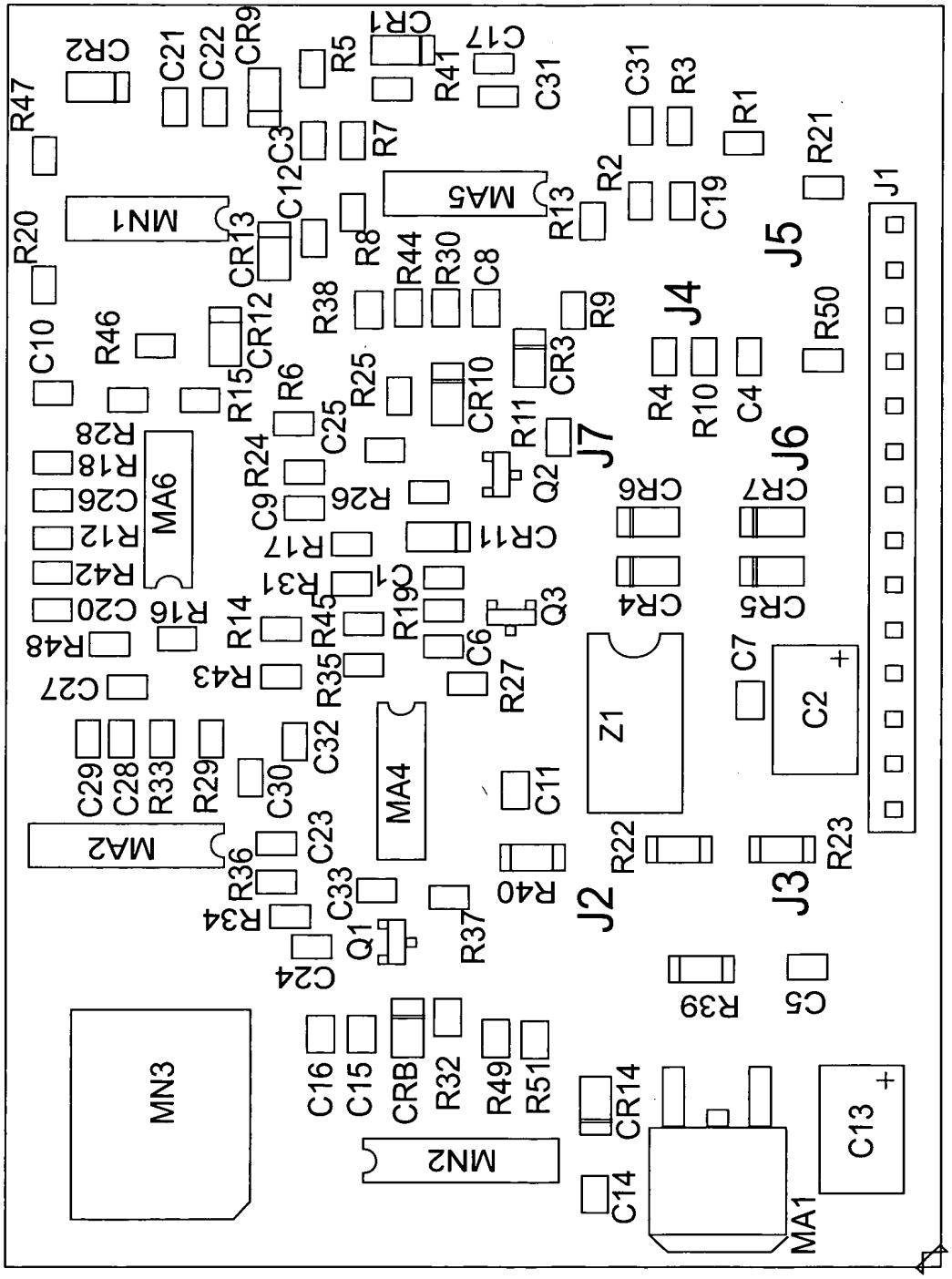
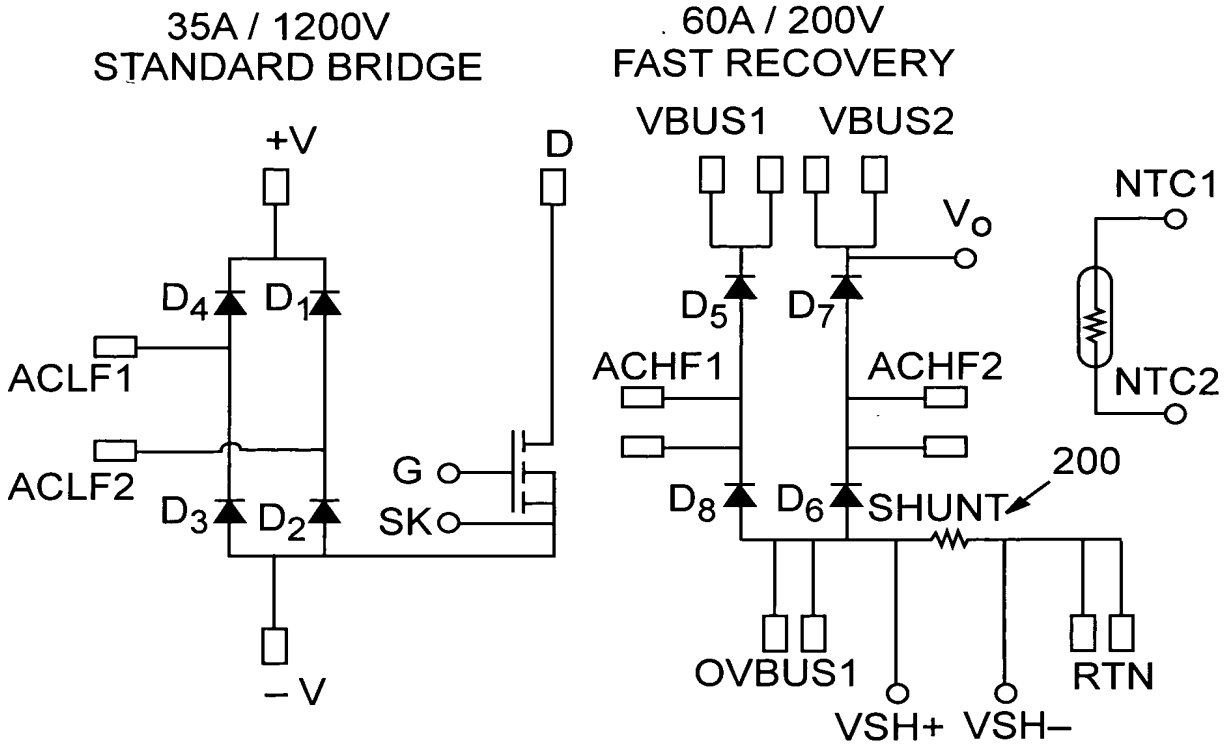


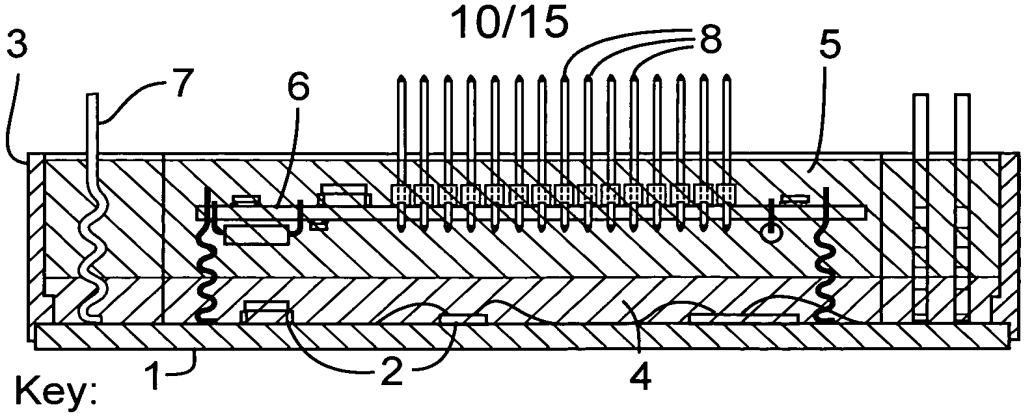
FIG. 10B POWER MODULE – LAYOUT
SMART CONVERTER MODULE – CONTROL STAGE



—o CONNECTION BETWEEN POWER SUBSTRATE AND PCB (INTERNAL CONNECTIONS)

—▭ POWER CONNECTION AVAILABLE TO USER

FIG. 11



Key:

(1) Module base plate (IMS substrate)
(2) Silicon chips and other power components, soldered to the substrate: upper connections to chips via ultrasonically bonded aluminum wires.
(3) Moulded outer wall
(4) Silicone gel conformal coating over substrate assembly
(5) Resin top layer to fill cavity
(6) Internal PCB, with all necessary control and protection functions: hybrid SMD/chip construction.
(7) 1 x 1.5 solderable power connectors
(8) Small signal connector. These connectors are available to the user for control circuit inputs (e.g. power supply points, DC output voltage feedback signal etc.)

FIG. 12 Cross Section of Module

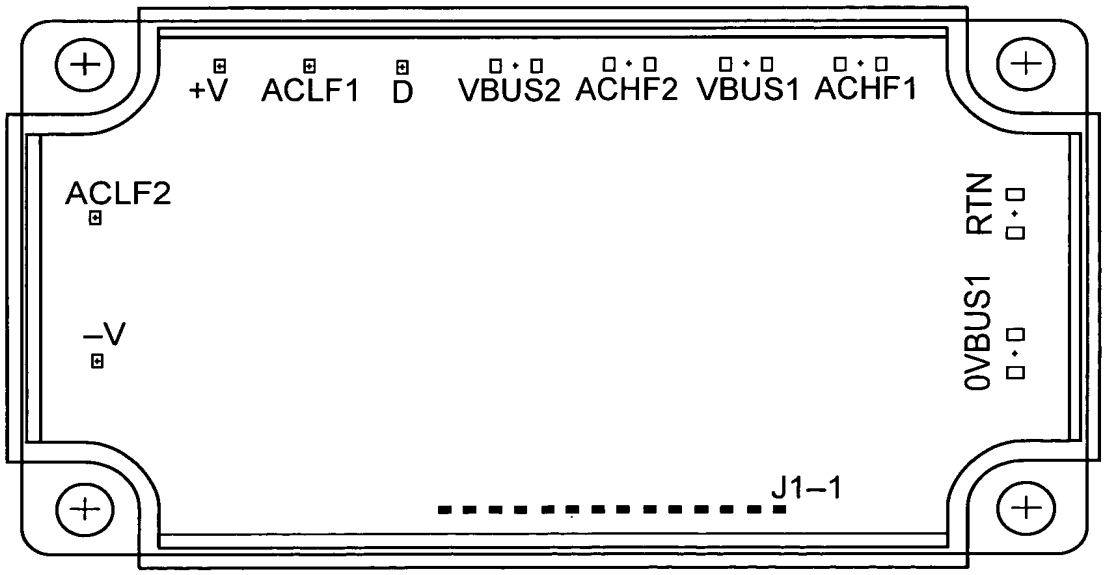


FIG. 13

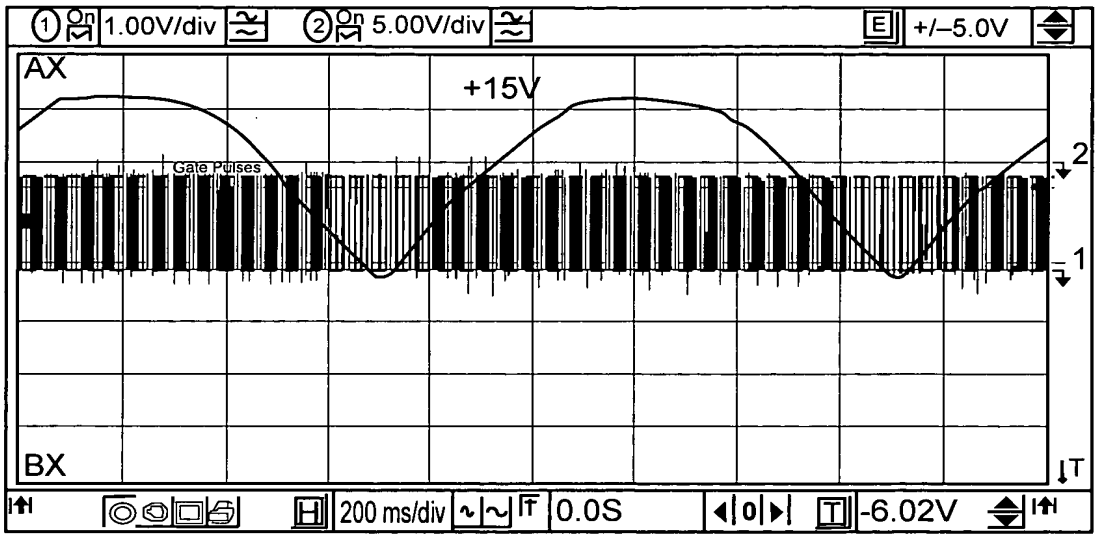

1.00V/div
5.00V/div
+/–5.0V
AX
+15V
Gate Pulses
BX
200 ms/div
0.0S
-6.02V

FIG. 14

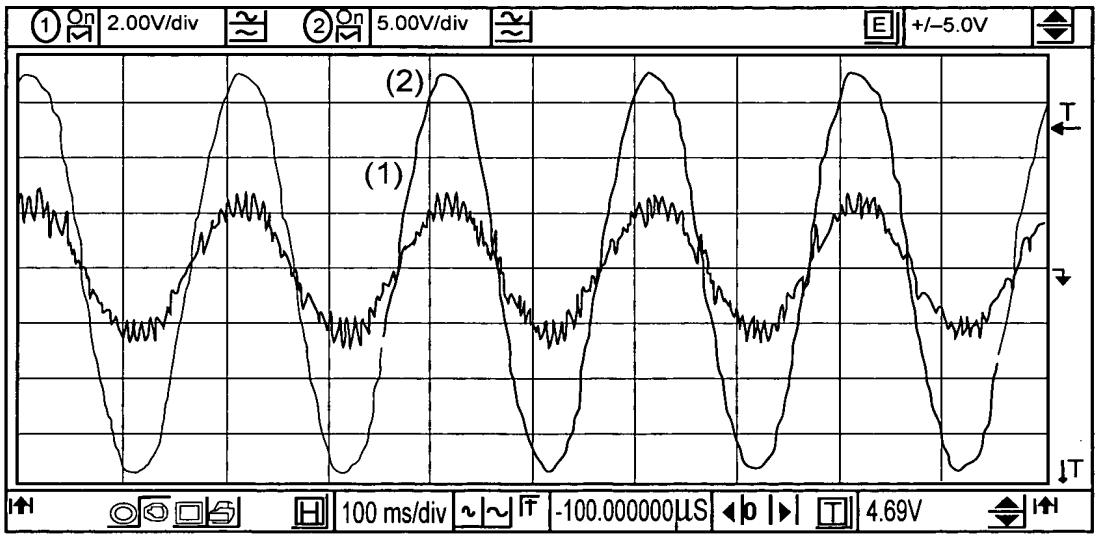

2.00V/div
5.00V/div
+/–5.0V
(2)
(1)
100 ms/div
-100.000000µS
4.69V

FIG. 15

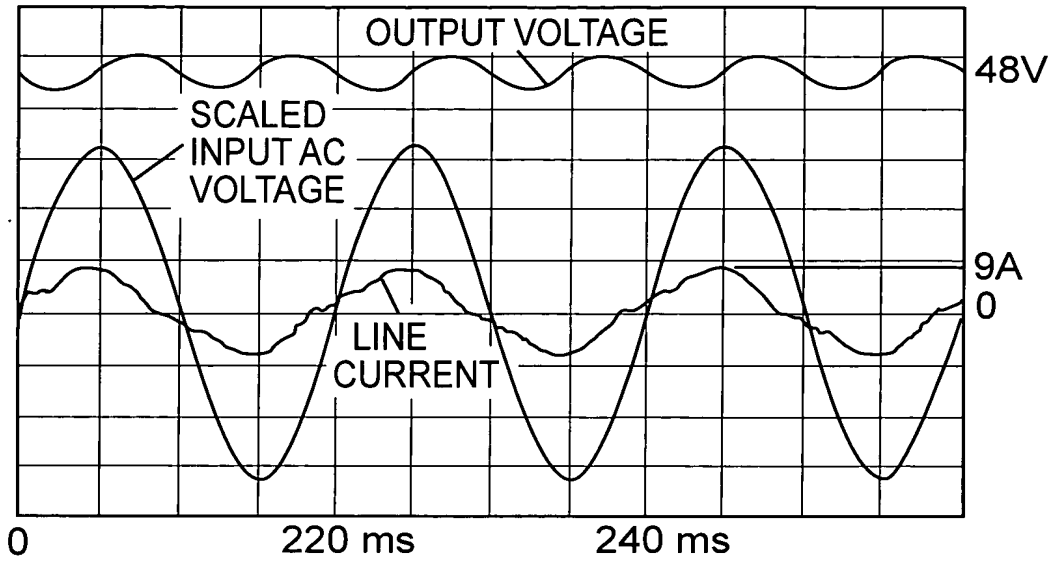


FIG. 16

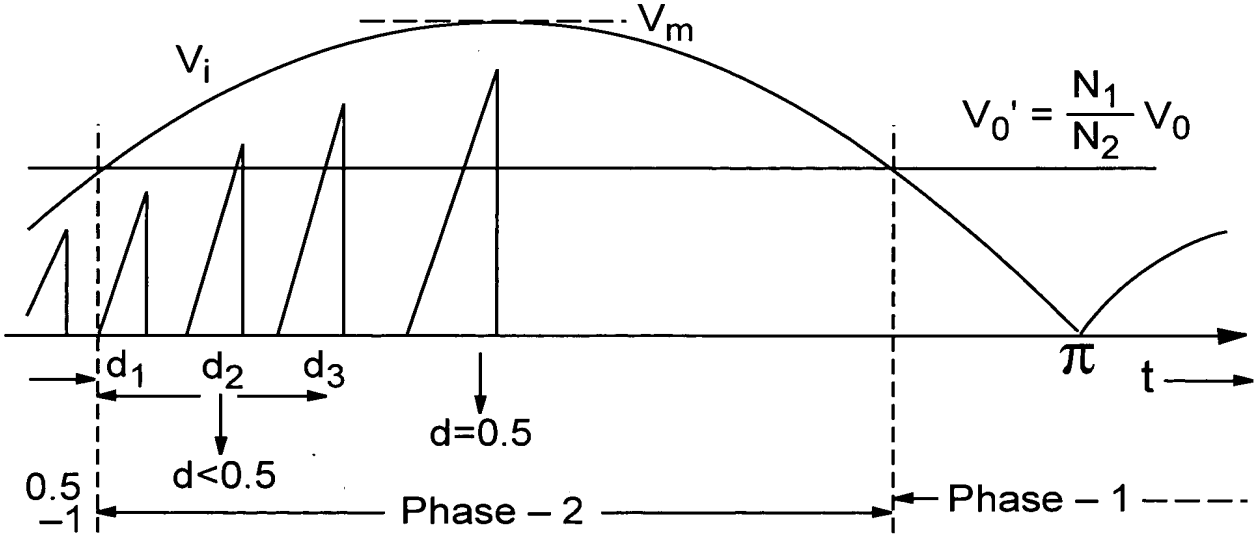


FIG. 17 Primary Side Current Waveforms Corresponding to the Maximum Load Condition $d_1 < d_2 < d_3 < \ldots\ldots$

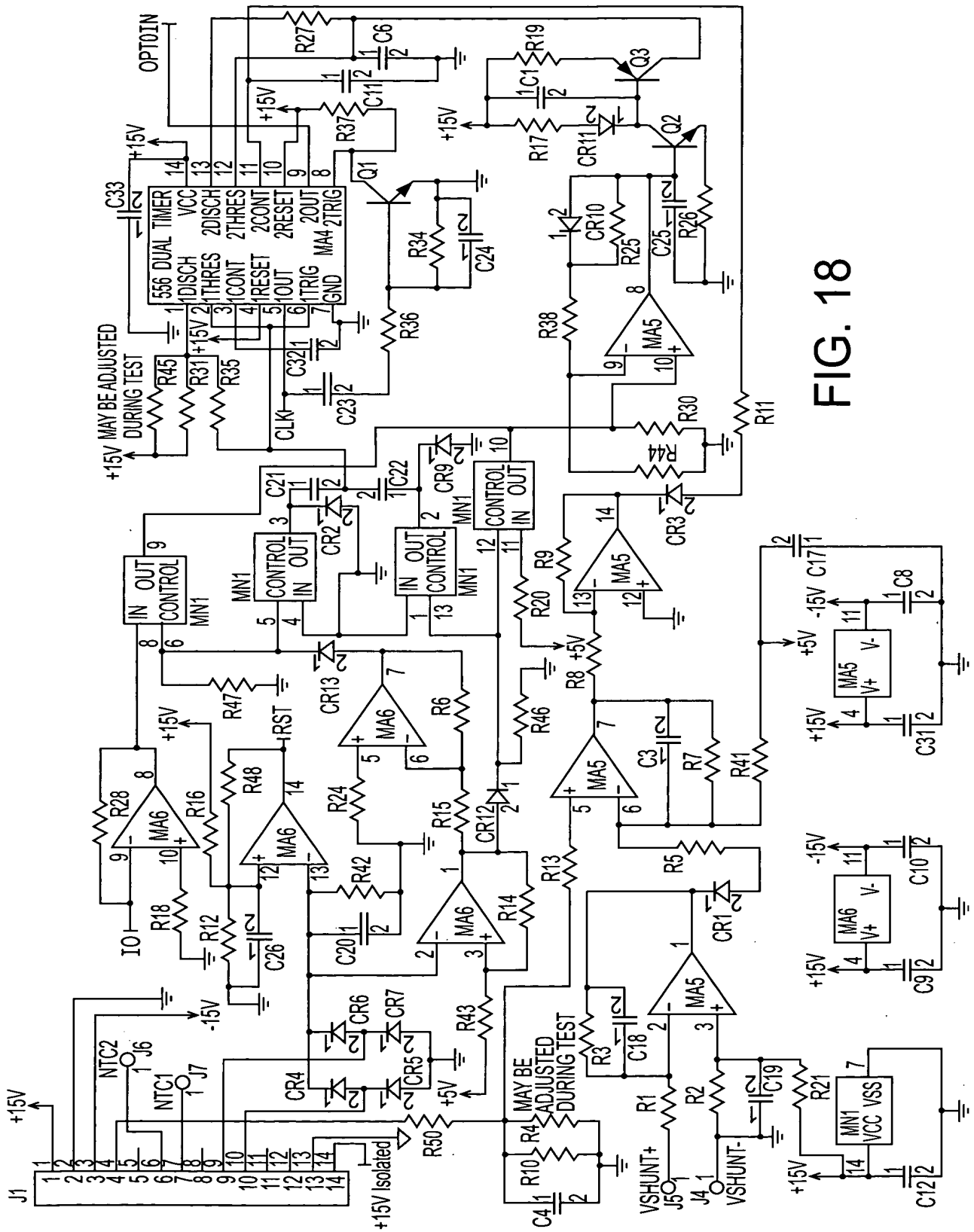

OPTOIN
+15V
556 DUAL TIMER
VCC
2DISCH
2THRES
2CONT
2RESET
2OUT
MA4
2TRIG
1DISCH
1THRES
1CONT
1RESET
1OUT
1TRIG
GND
MAY BE ADJUSTED DURING TEST
CLK
CONTROL
IN OUT
MN1
MA5
MA6
RST
IO
NTC2
NTC1
CR4
CR5
CR6
CR7
+15V Isolated
MAY BE ADJUSTED DURING TEST
VSHUNT+
VSHUNT-
-15V
+5V
MN1
VCC VSS
V+
V-

FIG. 18

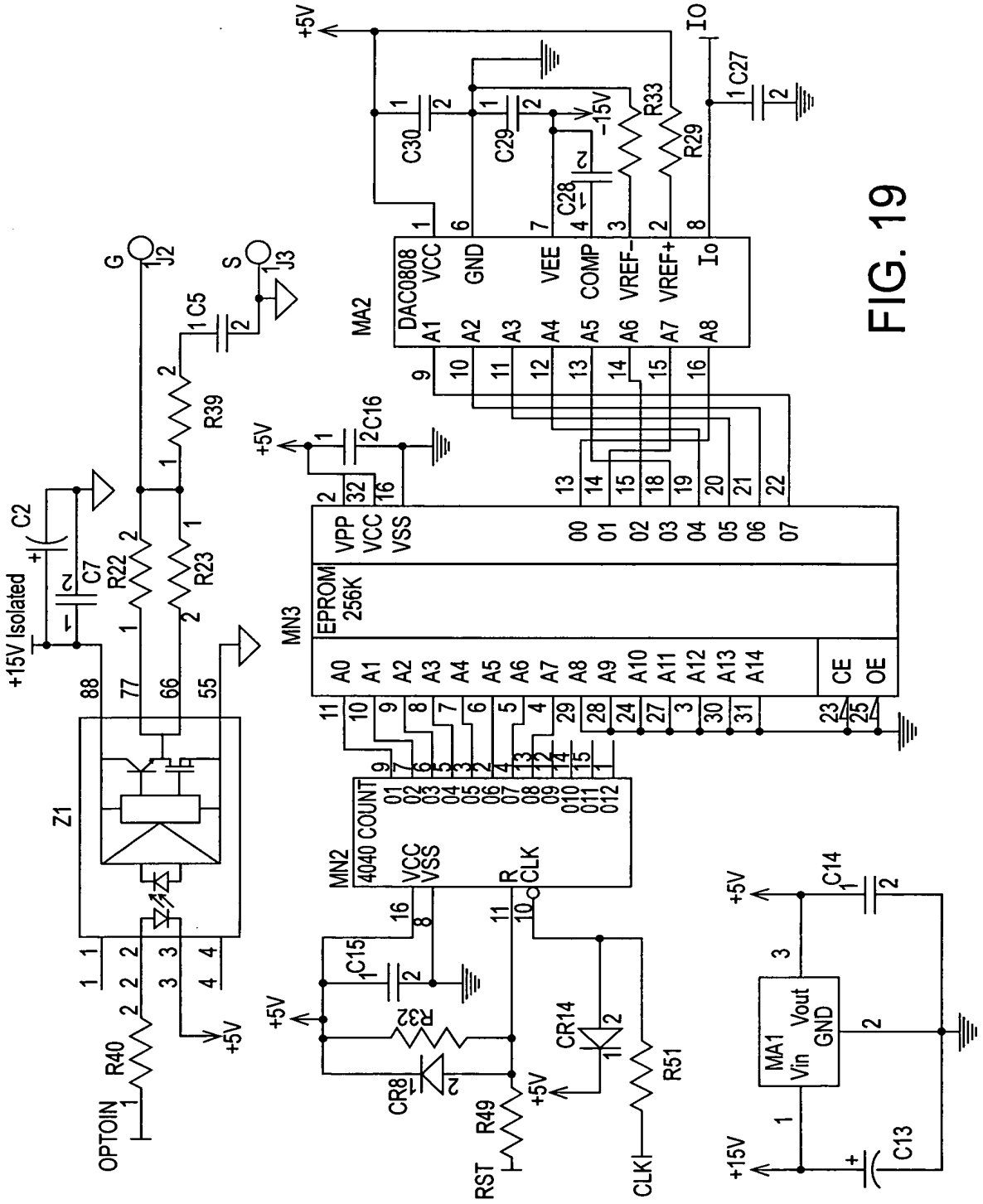

+5V
IO
C30
C29
C28
C27
R33
R29
-15V
DAC0808
VCC
GND
VEE
COMP
VREF-
VREF+
Io
MA2
G
S
J2
J3
C5
R39
C16
C2
C7
R22
R23
+15V Isolated
VPP
VCC
VSS
EPROM
256K
MN3
Z1
MN2
4040 COUNT
R
CLK
C15
R32
CR8
R49
RST
CR14
R51
CLK
OPTOIN
R40
MA1
Vin
Vout
GND
C14
C13

FIG. 19

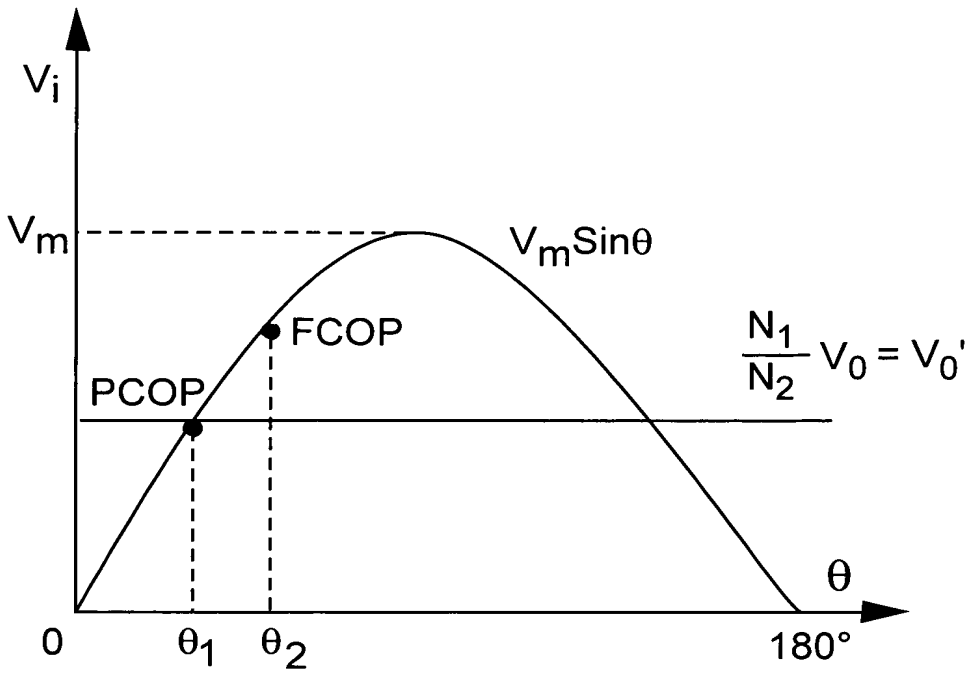


FIG. 20 Diagram showing relative positions of PCOP and FCOP